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- (71) Applicant (for all designated States except US): KONIN-KLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): CUPPENS, Roger [BE/BE]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). DITEWEG, Anthonie, M., H. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (74) Agent: ELEVELD, Koop, J.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

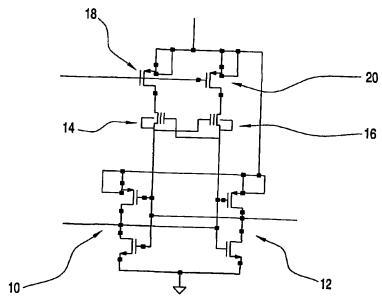
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(54) Title: NON-VOLATILE STATIC MEMORY CELL



(57) Abstract: A static memory cell comprising a pair of cross-coupled inverters (10, 12) which is "shadowed" with non-volatile memory elements (14, 16) so that data written in the static memory can be stored in the non-volatile cell, but also can be recalled later. The non-volatile cells (14, 16) are programmed with opposite data to increase the robustness of the retrieval process, and they are cross-coupled to the internal nodes (A, B) of the static memory cell, one the non-volatile cells (14) having a control gate connected to B and its source to A, and the other non-volatile element (16) having a control gate connected to A and its source to B. The drain of each non-volatile element (14, 16) is connected by means of a respective pMOS transistor (18, 20) to a program supply means.

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